

In the Claims:

Please amend the claims as follows:

1. (Original) A circuit comprising:
a reference signal;
a frequency synthesizer, receiving a dithered signal and the reference signal,
generating a constant frequency output; and
configuration registers transceiving data and control signals with the frequency synthesizer.
2. (Original) A circuit, as defined in claim 1, further comprising a modulated analog phase lock loop, receiving the reference signal, generating the dithered signal.
3. (Original) A circuit, as defined in claim 1, the frequency synthesizer comprising:
a predictor and corrector that receive the dithered signal and the reference signal,
generating a "remove pulse" signal; and
an output generator, receiving the dithered signal, reference signal, and "remove pulse" signal, generating a "clear pulse" signal and the constant frequency output.
4. (Original) A circuit, as defined in claim 1, the frequency synthesizer comprising:
a predictor, generating a first output signal indicative of the average number of dithered periods to remove per dithered period;
a corrector receiving the first output signal, generating a second output signal indicative of the fractional number of dithered periods to remove each dithered period; and
an accumulator receiving the second output signal, operative to count the fractional number of dithered periods, removing a dithered period when an integer has been reached.
5. (Original) A circuit, as defined in claim 4, the predictor comprising:
means for measuring the average number of dithered periods for the sample of the reference signal;

a comparator, receiving the first output signal and a desired number of dithered periods per sample of the reference signal, generating a difference indicative of the average number of dithered periods to remove per sample of the reference signal; and

a multiplier, receiving the difference, operative to scale the difference according to a scale factor register value.

6. (Original) A circuit, as defined in claim 4, the corrector comprising:
means for measuring error from the last sample;
means for determining a scale to fractional error; and
an adder, receiving the scale to fractional error and the average number of dithered periods to remove per dithered period, generating the difference.

7. (Currently Amended) A circuit, as defined in claim 1, the frequency synthesizer including:

a first synchronizer, receiving a system clock as reference input and a PLL output, and generating a first output;

an edge detector coupled to the first synchronizer to, receiving-receive the first output and the PLL output, and generating an edge signal;

a second synchronizer, adapted to receives an enable signal and the system clock and, generating a second output;

an adder configured to, receiving-receive reference count signals and, generating adder output signals;

an ~~Expected Count Latch~~ expected count latch coupled to the second synchronizer to, receiving-receive the second output as a clear input, receiving the system clock as a clock input, ~~the adder output signals~~ from the adder as data, and the edge signal as a load signal, and generating a latch output;

wherein the adder further receives the latch output;

an ~~Edge-edge Counter~~ counter coupled to the second synchronizer, the edge counter, receiving-receives the system clock and the second output as a clear signal and, generating-generates a counter output; and

a comparator coupled to the edge counter and the expected count latch and, receiving-receives the counter output and the latch output, and generating-generates a

rollover output, an $A > B + I$ signal, and an $A > B$ signal.

8. (Original) A method for frequency synthesis comprising:
receiving a dithered signal and a reference signal;
selecting a desired number of periods in the dithered signal to receive during a sample period of the reference signal;
counting the actual number of periods in the dithered signal during the sample period;
comparing the desired number to the actual number;
generating a constant frequency signal based on the comparison.

9. (Original) A method for frequency synthesis comprising:
receiving a dithered signal and a reference signal;
determining an average fractional number of dithered periods of the dithered signal to remove each dithered period;
determining a fractional error of dithered periods for each dithered period based on a period of the reference signal; and
combining the average fractional number and the fractional error generating a fractional number of dithered periods to remove each dithered period; and
generating a constant frequency signal based on the combination.

10. (Original) A method for frequency synthesis, as claimed in 9, determining an average fractional number of dithered periods comprising:
measuring an average number of dithered periods for a sample of the reference signal;
generating a difference from the average number of dithered periods and a desired number of dithered periods per sample of the reference signal, the difference indicative of the average number of dithered periods to remove per sample of the reference signal; and
scaling the difference according to a scale factor register value.

11. (Original) A method for frequency synthesis, as defined in claim 9, determining a fractional error of dithered periods for each dithered period comprising:

measuring error in a number of dithered periods corresponding to a given sample of the reference signal;

determining a scale to fractional error; and

scaling the scale to fractional error to generate the fractional error.

12. (Original) A method for frequency synthesis, as defined in claim 11, wherein determining a scale to fractional error comprises referring to a look-up table.

13. (Original) An apparatus for frequency synthesis comprising:
a predictor operative to estimate an average amount of correction per sample;
a corrector operative to measure actual error in a previous sample;
an accumulator, connected to the predictor and corrector, generating an accumulator output signal indicative of the sum of the average amount of correction and the actual error;
an output generator, receiving the accumulator output signal, generating an output signal having constant frequency.